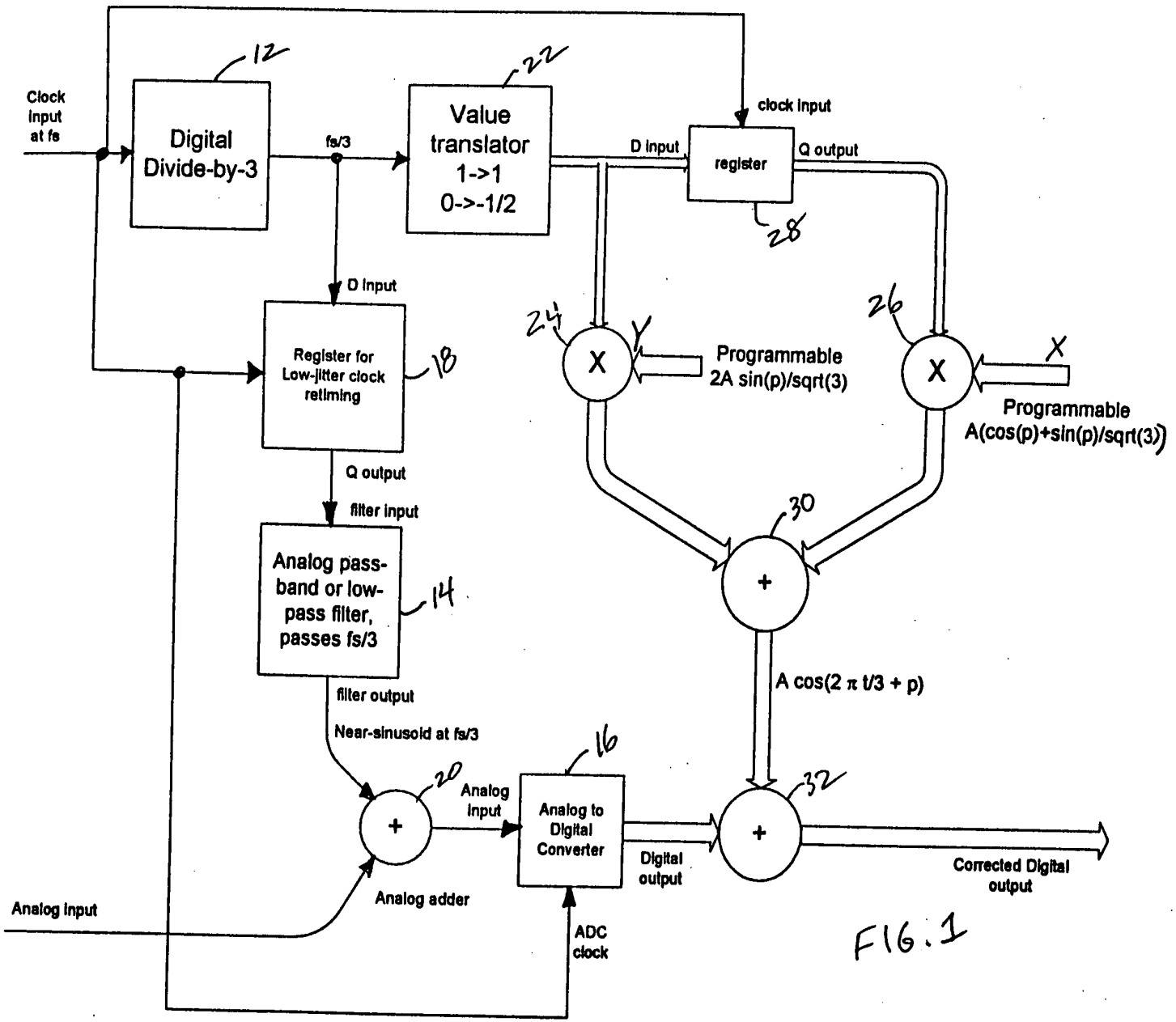
Clock input at fs
12
Digital Divide-by-3
fs/3
22
Value translator 1->1 0->-1/2
clock input
D input
register
Q output
28
D input
Register for Low-jitter clock retiming
18
24
X
Y
Programmable 2A sin(p)/sqrt(3)
26
X
X
Programmable A(cos(p)+sin(p)/sqrt(3))
Q output
filter input
Analog pass-band or low-pass filter, passes fs/3
14
30
+
A cos(2 π t/3 + p)
filter output
Near-sinusoid at fs/3
16
20
+
Analog input
Analog to Digital Converter
32
+
Digital output
Corrected Digital output
Analog input
Analog adder
ADC clock

FIG. 1